A 0.1-23-GHz SiGe BiCMOS Analog Multiplier and Mixer Based on Attenuation-Compensation Technique

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Abstract **— A SiGe BiCMOS broadband mixer and analog multiplier using LC ladder matching networks and attenuation-compensation method were first proposed. This broadband mixer achieves measured conversion gain of 19 dB with a 3-dB bandwidth from 0.1 to 23 GHz. The mixer was fabricated in a commercial 0.35-μm SiGe BiCMOS technology and demonstrated the highest gain-bandwidth product of operation among previously reported MMIC mixers. As an analog multiplier, the measured sensitivity is better than 3000 V/W from 0.1 to 25 GHz with 50-Ω output impedance. The chip area is 1.5 x 1 mm² including testing pad. The performance of this circuit represents state-of-the-art result of the MMIC broadband mixers using standard silicon-based technologies.**

Index Terms **— Monolithic microwave integrated circuits, heterojunction bipolar transistors, silicon, broadband communication, mixers.**

I. INTRODUCTION

The Gilbert-cell multipliers and mixers have been demonstrated with various monolithic microwave integrated circuit (MMIC) technologies [1]-[16]. Record mixer RF bandwidth has been demonstrated using 0.1-μm InP high electron-mobility transistor (HEMT) technology with low gain [2]. With high f_T (70 GHz), the InP HBT-based analog mixer has demonstrated a record gain-bandwidth product (GBP) of 116.4 GHz [19]. The highest operation frequency of reported broadband active mixer was demonstrated using a f_{MAX} of 128 GHz SiGe-HBT process, but it fall short of providing operation frequency below 12 GHz [10]. With broadband input transmission-line matching networks, medium conversion gain of mixer from 1 to 17 GHz in InGaP-GaAs HBT technology has been presented in [6].

In this study, we demonstrated a wide-bandwidth 0.1-23-GHz SiGe BiCMOS analog multiplier and mixer. This active mixer is based on the Gilbert transconductance multiplier cell. Although the f_{MAX} of the device used in the design is about 57 GHz, significantly lower than that of the GaAs, SiGe, and InP HBT device, our LC ladder matching networks and attenuation-compensation method resulted in high gain and wide bandwidth for this chip. The MMIC chip without RF, LO, IF amplifiers also shows high frequency-conversion performance compared with those of GaAs, SiGe, and InP HBT analog multipliers and mixers. Fig. 1 summarizes published wide-band mixer integrated-circuit (IC) gain and bandwidth performance. Our SiGe BiCMOS MMIC achieves a measured conversion gain of 19 dB and 3-dB bandwidth from 0.1 to 23 GHz and, thus, even without a pre- or post-amplifier, gives the highest gain-bandwidth product of 204 GHz among the reported SiGe, InP and GaAs-based HBT analog active mixer.

Process	f_T/f_{max} (GHz)	Design Topology	Gain (dB)	Bandwidth (GHz)	GBP (GHz)	Ref.
GaAs HBT	90/70	Gilbert Cell	5	DC to 20	35.5	[1]
InP HEMT	155/-	Distributed mixer	-5	DC to 38	21.4	[2]
InP HBT	90 / 70	Gilbert cell with LO drive and IF buffer	-6	DC to 15	8	[3]
GaAs HBT	40 /140	Gilbert cell with TL-matching network	9.3	1 to 17	45	[6]
GaAs HBT	-	Gilbert micromixer	11	DC to 8	28.4	[9]
Si BJT	20 /-	Gilbert Cell	15	DC to 8	45	[11]
Si BJT	10/20	Gilbert Cell	16	DC to 6	37.8	[13]
SiGe HBT	80/97	Gilbert Cell	5.9	2 to 30	55.2	[14]
SiGe HBT	80/97	Gilbert Cell	10	1 to 20	60	[15]
InP HBT	70 / 160	Gilbert cell with LO, RF and IF amplifier	15	DC to 20	116.4	[16]
SiGe BiCMOS	80 / 57	Gilbert Cell with attenuation compensation and LC ladder matching network	19	0.1 to 23	204	This Work

Fig. 1. Comparison of monolithic integrated mixers in various MMIC technologies

II. MMIC PROCESS

The broadband mixer was designed using TSMC commercial 0.35-μm 3P3M SiGe BiCMOS technology, which provides three poly layers for the emitters and bases of the SiGe heter-junction bipolar transistor (HBT) and the gates of the complementary MOS (CMOS) transistors; three metal layers for inter-connection. The HBT manufactured in this technology offer cut-off frequency of 80 GHz, maximum oscillation frequency of 57 GHz. Unlike the high-resistivity substrate of SiGe HBT process, the SiGe BiCMOS process with low-resistivity substrate provides monolithic inductors with quality factor below 10. A MIM capacitor of 1fF/mm² has been developed using oxide inter-metal dielectric. Polysilicon resistors, with several Ω/• and kΩ/•, are provided by choosing the individual dose of ion-implantation separately form the gate electron doping process.

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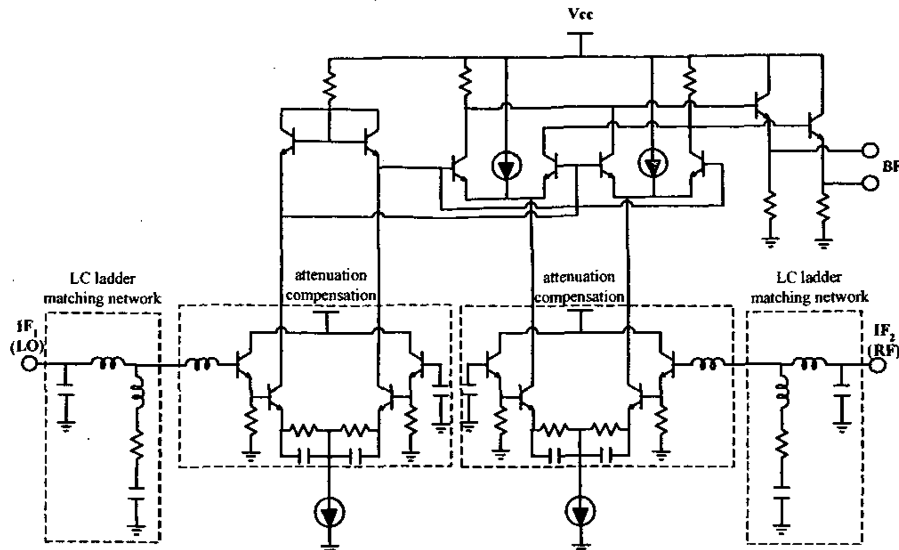

Fig. 2. Circuit schematic of the SiGe BiCMOS broadband mixer/multiplier

III. CIRCUIT DESIGN

The circuit schematic of this broadband mixer/multiplier is shown in Fig. 2. The circuit can be divided into the: 1) predistortion circuit; 2) dc-bias circuit; 3) output buffer; 4) Gilbert cell core; 5) input LC ladder matching network; 6) attenuation-compensation circuit. The Gilbert cell configuration is selected for the double balanced implementation which offers high conversion gain and improved spur performance in a very compact size [1]. The RF signal enters a lower amplifier formed by the emitter coupled pair. The LO signal enters an upper cross coupled quad of devices through the predistortion circuit.

In order to improve the bandwidth, wideband impedance match is necessary for reducing signal reflection. Wideband impedance match can be achieved by equivalent 50-Ω resistors shunted with the high input impedances of the input transistors in previous existing designs [1], but the capacitive-looking impedance of the emitter couple pairs (ECPs) at upper band edge will degrade the return loss [6]. Moreover, the shunt resistor deteriorates the conversion gain at high frequency. Broadband analog multiplier/mixer adopted transmission-line matching networks achieved better conversion gain and input return loss simultaneously than that in equivalent shunted 50-Ω resistors [5].

However, the base parasitic resistance (R_B) of HBT transistors is generally larger than that of FETs depends on the transistor size [18]. The base resistance (R_B) increases the loss of the artificial transmission line formed by the LC ladder matching network. Moreover, the monolithic inductors in standard silicon substrate suffer more loss than that in GaAs or InP technology. These energy losses will degrade the overall performance of wideband mixer and multiplier, e.g. bandwidth and conversion gain, etc. In order to promote to high frequency performance in standard silicon technology, the attenuation-compensation method is adopted to overcome these obstacles.

The attenuation-compensation network consists of Darlington (CC-CE) configuration, and the LC ladder matching networks, as shown in Fig. 2, are adopted to implement the wideband impedance matching which is generally used in distributed circuits. The matching network is loaded by the input equivalent capacitance of attenuation-compensation network and is terminated in its characteristic impedance at the end with spiral inductors to perform an artificial transmission line. All the passive elements of capacitors and inductors are simulated by the full-wave simulation tool [17] to predict the high frequency effects. Fig. 3 shows the chip micrograph with a chip size of 1.5 × 1 mm^2.

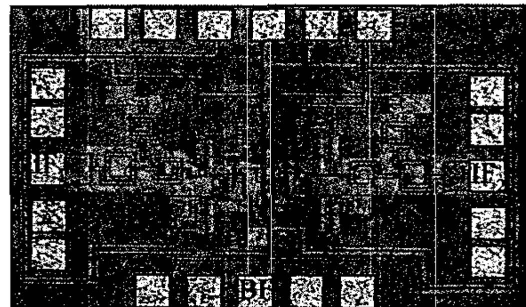
Fig. 3. Chip micrograph (size: 1.5 mm × 1 mm)

IV. MEASUREMENT RESULTS

The mixer characteristics of the chip were measured using on-wafer probing on IF_1 as LO input port and IF_2 as RF input ports with ground-signal-ground (GSG) probes. While measuring the multiplier characteristics, the input signals were fed from the IF pads and the output was extracted from the BF pad. This chip was measured using wire bonding of output pads as the output port (indicated as BF in Fig. 3). The output was then connected to a spectrum analyzer through dc-blocking capacitors. Fig. 4 shows the conversion gain as a function of LO power with RF frequency of 10 GHz and IF frequency of 10 MHz. It shows that the conversion gain almost saturated approximately 0 dBm of LO power. The conversion gain versus the RF frequency is shown in Fig. 5 with both RF and LO ports swept in frequency up to 30 GHz, a fixed IF frequency of 10 MHz, and LO power of -1 dBm. The conversion gain is approximately 19 dB with a 3-dB bandwidth of 23 GHz from 0.1 to 23 GHz.

The multiplier characteristics were measured with the same setup as the mixer measurement. The output voltage versus the IF frequency is shown in Fig. 6, with two IF ports swept in frequency from 0.1 to 30 GHz, a fixed baseband frequency (BF) of 10 MHz, and IF power of -20 dBm. The sensitivity, which is the ratio of BF output voltage to total IF input power, was better than 3000 V/W with a bandwidth of 0.1-25 GHz. Total power consumption is 145 mW.

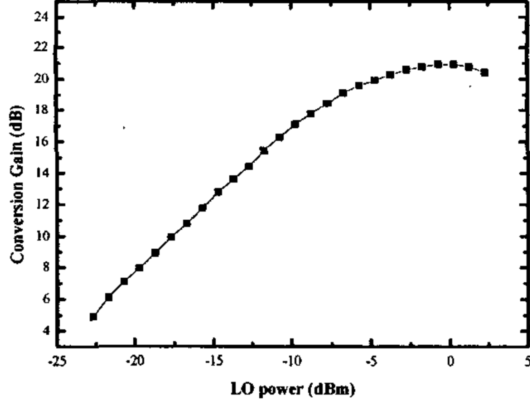

Fig. 4. The measured conversion gain versus LO input power at RF frequency of 10 GHz

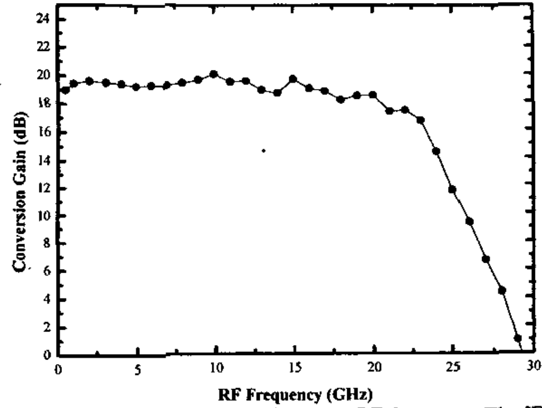

Fig. 5. Measured conversion gain versus RF frequency. The IF frequency 10 MHz, LO power is 0 dBm.

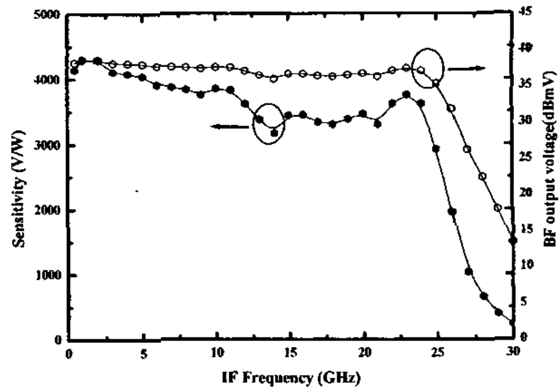

Fig. 6. Measured BF output voltage with IF power of -20 dBm and sensitivity from 0 to 30 GHz

V. CONCLUSION

An active broadband analog multiplier and mixer in commercial 0.35-μm SiGe BiCMOS technology has been presented. The mixer sets state-of-the-art for monolithic integrated mixers realized in standard silicon technologies. The LC ladder matching networks are used to achieve broadband impedance matching, and the attenuation-compensation method is also adopted to promote the conversion gain and bandwidth. A high conversion gain of 19 dB is achieved with a 3-dB bandwidth of 0.1-23 GHz. The highest gain-bandwidth product of 204 GHz among the reported SiGe, InP and GaAs-based HBT analog active mixer is also achieved. Since the broadband mixer/multiplier was fabricated in standard silicon technology, it can be easily integrated with other Si-based front-end circuits without requiring any post-processing steps.

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